REMARKS/ARGUMENT

Claims 1-4, 16-21 and 32-36 stand rejected under 35 U.S.C. 102(b) as being anticipated by European patent Application 0153107 (hereinafter "Hogan"). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1-4, 16-21 and 32-36 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

(A) Independent Claim 1 requires and positively recites, a **transmit filter** for **generating an oversampled signal** from a stream of data symbols generated responsive to a symbol clock, comprising: "circuitry for receiving the data symbol stream" , "**phase tracking circuitry**, responsive to a **reference clock generated independently from the symbol clock**, for maintaining phase information relative to the symbol clock" and "**sample generating circuitry** for generating samples **responsive to said phase information**".

In contrast, Hogan (EU patent application 0153107) discloses "a clock recovery apparatus 10" that "receives an input data stream (...) 12", feeds it to "a phase comparison circuitry 16", which measures "the phase difference between the data stream input (...) 22"

and "the clock generator output (...) 20". The "decision circuitry 24" "provides a phase selection signal (...) 28" to adjust the phase of "the clock generator 18" (Page 5). The apparatus in fact provides "a recovery of the clock from the incoming data stream" through the use of a "delay locked loop".

The present invention differs substantially from Hogan's in the following ways:

First, Hogan teaches only a clock recovery apparatus. He does not teach or suggest "a **transmit filter** ...", as required by Claim 1.

Second, Hogan teaches generating and outputting a digital stream that is merely a cleaner version of the input stream: "The resulting digital data stream from output circuitry 30 (...) thus corresponds to the input data stream with the amplitude noise eliminated and phase distortion reduced." Hence, a single-bit data stream input 12 produces a single-bit data stream output 32. Hogan does not teach or suggest, "**generating an oversampled signal** from a stream of data symbols generated responsive to a symbol clock", as further required by Claim 1.

Third, Hogan does not teach or suggest that the generated output to be samples. As such, Hogan fails to teach or suggest, "'**sample generating circuitry** for generating samples", as required by Claim 1.

Fourth, the clock recovery apparatus in Hogan attempts to follow the phase of the input data and to make necessary corrections: "The resulting clock transitions provided from the clock generator output line 20 should be as close as possible to the center of each bit cell and should be constantly correcting for the position of this center to maintain the clock transition to that center" (pp. 6, lines 10—15). This is the key and enabling feature of Hogan's invention. In contrast, the present invention does not perform this constant

correction of the clock transitions. The "constant correction" in Hogan is the direct result of using a "delay locked loop" (pp. 6, line 8). The present invention, on the other hand, does not employ any delay locked loop or any other constant feedback mechanism, other than a primitive digital accumulator 106 on Figure 8a.

Fifth, the output data stream 32 in Hogan is produced by the "output circuitry 30", which is a "clocked flip-flop" (pp. 11, line 25), which samples the input data stream with the clock generated by the clock generator 18. In contrast, the output data of the present invention is not a clocked version of the input data but is a result of complex digital filtering.

Moreover, in addition to the above reasons set forth in support of the allowance of Claim 1, which are sufficient by themselves to overcome the 35 U.S.C. 102(b) rejection of Claim 1 over Hogan, the Examiner's equating of elements in Hogan to the present invention is not correct. Examiner equates Hogan's clock recovery apparatus 10 with "transmit filter" in Claim 1. Examiner equates "circuitry for receiving the data symbol stream" element with Hogan's "input circuitry 14"and "phase comparison circuitry 16" that receive "an input data stream over a line 12". Examiner also equates "phase tracking circuitry" element with Hogan's "decision circuitry 24". Examiner further equates "sample generating circuitry" element with Hogan's "output circuitry 30". The "reference clock" in the second element is equated with the "clock generator 18" output 20. There is an implicit equating of "symbol clock" to the original clock used to generate the input data stream 12 in Hogan. The interpretation of Hogan set forth by the Examiner will not work for several reasons:

1. "Phase tracking circuitry" element assumed now 24 is <u>not</u> "responsive to a reference clock" now assumed 20. In Hogan, clock 20 is input to circuit 16, which Examiner equated to Claim 1's "circuitry for receiving the data symbol stream".

For this assumption to stand in Hogan, clock 20 would instead need to be input to circuit 24, which breaks the operation.

2. The "reference clock" in the second element is not "generated independently from the symbol clock". It is the objective of Hogan's invention to continuously adjust the phase of clock 20 to the input data (see Fourth point hereinabove). Hence, by virtue of proper operation, Hogan's invention cannot provide the "reference clock generated independently from the symbol clock."

3. The "sample generating circuitry" element assumed now 30 is not "responsive to said phase information". In Hogan, the circuit 30 is connected to only the input data 22 and generated clock 20, not the signal 28, Examiner has equated with "phase information" signal.

Accordingly, the 35 U.S.C. 102(b) rejection of Claim 1 is improper and must be withdrawn.

(b) Independent Claim 18 requires and positively recites, a method of **generating a oversampled signal** from a stream of data symbols generated responsive to a symbol clock, comprising the steps of: "receiving the data symbol stream", "maintaining phase information relative to **the symbol clock in response to a reference clock generated independently from the symbol clock**" and "generating samples **responsive to said phase information** and said reference clock".

In contrast, Hogan (EU patent application 0153107) discloses "a clock recovery apparatus 10" that "receives an input data stream (...) 12", feeds it to "a phase comparison

circuitry 16", which measures "the phase difference between the data stream input (...) 22" and "the clock generator output (...) 20". The "decision circuitry 24" "provides a phase selection signal (...) 28" to adjust the phase of "the clock generator 18" (Page 5). The apparatus in fact provides "a recovery of the clock from the incoming data stream" through the use of a "delay locked loop".

The present invention differs substantially from Hogan's in the following ways:

First, Hogan teaches generating and outputting a digital stream that is merely a cleaner version of the input stream: "The resulting digital data stream from output circuitry 30 (...) thus corresponds to the input data stream with the amplitude noise eliminated and phase distortion reduced." Hence, a single-bit data stream input 12 produces a single-bit data stream output 32. Hogan does not teach or suggest, "**generating an oversampled signal** from a stream of data symbols generated responsive to a symbol clock", as required by Claim 18.

Second, Hogan does not teach or suggest that the generated output to be samples. As such, Hogan fails to teach or suggest, "**generating samples** responsive to said phase information ...", as further required by Claim 18.

Third, the output data stream 32 in Hogan is produced by the "output circuitry 30", which is a "clocked flip-flop" (pp. 11, line 25), which samples the input data stream with the clock generated by the clock generator 18. In contrast, the output data of the present invention is not a clocked version of the input data but is a result of complex digital filtering. As such, Hogan fails to teach or suggest, "maintaining phase information relative to **the symbol clock in response to a reference clock generated independently from the symbol clock**", as required by Claim 18.

Fourth, the clock recovery apparatus in Hogan attempts to follow the phase of the input data and to make necessary corrections: "The resulting clock transitions provided from the clock generator output line 20 should be as close as possible to the center of each bit cell and should be constantly correcting for the position of this center to maintain the clock transition to that center" (pp. 6, lines 10—15). This is the key and enabling feature of Hogan's invention. In contrast, the present invention does not perform this constant correction of the clock transitions. The "constant correction" in Hogan is the direct result of using a "delay locked loop" (pp. 6, line 8). The present invention, on the other hand, does not employ any delay locked loop or any other constant feedback mechanism, other than a primitive digital accumulator 106 on Figure 8a.

Moreover, in addition to the above reasons set forth in support of the allowance of Claim 18, which are sufficient by themselves to overcome the 35 U.S.C. 102(b) rejection over Hogan, the Examiner's equating of elements in Hogan to the present invention is not correct. Examiner equates Hogan's clock recovery apparatus 10 with "transmit filter" in Claim 1. Examiner equates "circuitry for receiving the data symbol stream" element with Hogan's "input circuitry 14"and "phase comparison circuitry 16" that receive "an input data stream over a line 12". Examiner also equates "phase tracking circuitry" element with Hogan's "decision circuitry 24". Examiner further equates "sample generating circuitry" element with Hogan's "output circuitry 30". The "reference clock" in the second element is equated with the "clock generator 18" output 20. There is an implicit equating of "symbol clock" to the original clock used to generate the input data stream 12 in Hogan. The interpretation of Hogan set forth by the Examiner will not work for several reasons:

4. "Phase tracking circuitry" element assumed now 24 is not "responsive to a reference clock" now assumed 20. In Hogan, clock 20 is input to circuit 16, which Examiner equates to Claim 18's "receiving the data symbol stream". For this

assumption to stand in Hogan, clock 20 would instead need to be input to circuit 24, which breaks the operation.

5. The "reference clock" in the third step element is not "generated independently from the symbol clock". It is the objective of Hogan's invention to continuously adjust the phase of clock 20 to the input data (see Fourth point hereinabove). Hence, by virtue of proper operation, Hogan's invention cannot provide the "reference clock generated independently from the symbol clock.", as required by Claim 18.

6. The "generating samples ..." step presumed by the Examiner 30 in Hogan is not "responsive to said phase information". In Hogan, the circuit 30 is connected to only the input data 22 and generated clock 20, not the signal 28, Examiner has equated with "phase information" signal.

Accordingly, the 35 U.S.C. 102(b) rejection of Claim 18 is improper and must be withdrawn.

(C) Independent Claim 34 requires and positively recites, a **transmit filter** for **generating a oversampled signal** from a stream of data symbols generated responsive to a symbol clock, comprising: "circuitry for receiving the data symbol stream", "**phase tracking circuitry**, responsive to a **reference clock**, for maintaining phase information relative to the symbol clock" and "sample generating circuitry for selectively generating samples **responsive to said phase information** and said symbol clock".

In contrast, Hogan (EU patent application 0153107) discloses "a clock recovery apparatus 10" that "receives an input data stream (...) 12", feeds it to "a phase comparison

circuitry 16", which measures "the phase difference between the data stream input (...) 22" and "the clock generator output (...) 20". The "decision circuitry 24" "provides a phase selection signal (...) 28" to adjust the phase of "the clock generator 18" (Page 5). The apparatus in fact provides "a recovery of the clock from the incoming data stream" through the use of a "delay locked loop".

The present invention differs substantially from Hogan's in the following ways:

First, Hogan teaches only a clock recovery apparatus. He does not teach or suggest "a **transmit filter** ...", as required by Claim 34.

Second, Hogan teaches generating and outputting a digital stream that is merely a cleaner version of the input stream: "The resulting digital data stream from output circuitry 30 (...) thus corresponds to the input data stream with the amplitude noise eliminated and phase distortion reduced." Hence, a single-bit data stream input 12 produces a single-bit data stream output 32. Hogan does not teach or suggest, "**generating an oversampled signal** from a stream of data symbols generated responsive to a symbol clock", as further required by Claim 34.

Third, Hogan does not teach or suggest that the generated output to be samples. As such, Hogan fails to teach or suggest, "'**sample generating circuitry** for generating samples", as required by Claim 34.

Fourth, the clock recovery apparatus in Hogan attempts to follow the phase of the input data and to make necessary corrections: "The resulting clock transitions provided from the clock generator output line 20 should be as close as possible to the center of each bit cell and should be constantly correcting for the position of this center to maintain the clock transition to that center" (pp. 6, lines 10—15). This is the key and enabling feature

of Hogan's invention. In contrast, the present invention does not perform this constant correction of the clock transitions. The "constant correction" in Hogan is the direct result of using a "delay locked loop" (pp. 6, line 8). The present invention, on the other hand, does not employ any delay locked loop or any other constant feedback mechanism, other than a primitive digital accumulator 106 on Figure 8a.

Moreover, in addition to the above reasons set forth in support of the allowance of Claim 34, which are sufficient by themselves to overcome the 35 U.S.C. 102(b) rejection of Claim 34 over Hogan, the Examiner's equating of elements in Hogan to the present invention is not correct. Examiner equates Hogan's clock recovery apparatus 10 with "transmit filter" in Claim 34. Examiner equates "circuitry for receiving the data symbol stream" element with Hogan's "input circuitry 14"and "phase comparison circuitry 16" that receive "an input data stream over a line 12". Examiner also equates "phase tracking circuitry" element with Hogan's "decision circuitry 24". Examiner further equates "sample generating circuitry" element with Hogan's "output circuitry 30". The "reference clock" in the second element is equated with the "clock generator 18" output 20. There is an implicit equating of "symbol clock" to the original clock used to generate the input data stream 12 in Hogan. The interpretation of Hogan set forth by the Examiner will not work for several reasons:

7. "Phase tracking circuitry" element assumed now 24 is not "responsive to a reference clock" now assumed 20. In Hogan, clock 20 is input to circuit 16, which Examiner equated to Claim 34's "circuitry for receiving the data symbol stream". For this assumption to stand in Hogan, clock 20 would instead need to be input to circuit 24, which breaks the operation.

8. The "reference clock" in the second element is not "generated independently from the symbol clock". It is the objective of Hogan's invention to continuously adjust

the phase of clock 20 to the input data (see Third point hereinabove). Hence, by virtue of proper operation, Hogan's invention cannot provide the "reference clock generated independently from the symbol clock."

9. The "sample generating circuitry" element assumed now 30 is not "responsive to said phase information". In Hogan, the circuit 30 is connected to only the input data 22 and generated clock 20, not the signal 28, Examiner has equated with "phase information" signal.

Accordingly, the 35 U.S.C. 102(b) rejection of Claim 34 is improper and must be withdrawn.

Claims 2-4, 16, 17, 19-21, 32, 33, 35 and 36 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the transmit filter of claim 1 wherein said sample generating circuitry generates samples at an active edge of said reference clock. Claim 2 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 3 further defines the transmit filter of claim 2 wherein said sample generating circuitry generates samples on each clock cycle of said reference clock. Claim 3 depends from Claim 2 and is therefore allowable for the same reasons set forth above for the allowance of Claim 2.

Claim 4 further defines the transmit filter of claim 2 wherein said sample generating circuitry generates samples on selected clock cycles of said reference clock.

Claim 4 depends from Claim 2 and is therefore allowable for the same reasons set forth above for the allowance of Claim 2. Moreover, and contrary to the Examiner's assertion, Rasmussen does not teach or suggest "generating samples on selected clock cycles of said reference clock." Column 4, lines 44—47 describes generating samples on ALL clock cycles of the reference clock (CLK1, which is generated by the timing and control circuit 29 in response to the NCO clock 17 output).

Claim 16 further defines the transmit filter of claim 1 and further comprising circuitry for identifying an approximate center of a data symbol. Claim 16 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 17 further defines the transmit filter of claim 16 and further comprising circuitry for tracking an approximate center for each data symbol in said stream independent of the symbol clock. Claim 17 depends from Claim 16 and is therefore allowable for the same reasons set forth above for the allowance of Claim 16.

Claim 19 further defines the method of claim 18 wherein said sample generating step comprises the step of generating samples at an active edge of said reference clock. Claim 19 depends from Claim 18 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18.

Claim 20 further defines the method of claim 19 wherein said sample generating step comprises the step of generating samples on each clock cycle of said reference clock. Claim 20 depends from Claim 19 and is therefore allowable for the same reasons set forth above for the allowance of Claim 19.

Claim 21 further defines the method of claim 19 wherein said sample generating step comprises the step of generating samples on selected clock cycles of said reference clock. Claim 21 depends from Claim 19 and is therefore allowable for the same reasons set forth above for the allowance of Claim 19.

Claim 32 further defines the method of claim 18 and further comprising the step of identifying an approximate center of a data symbol. Claim 32 depends from Claim 18 and is therefore allowable for the same reasons set forth above for the allowance of Claim 18.

Claim 33 further defines the method of claim 32 and further comprising the step of tracking an approximate center for each data symbol in said stream independent of the symbol clock. Claim 33 depends from Claim 32 and is therefore allowable for the same reasons set forth above for the allowance of Claim 32.

Claim 35 further defines the transmit filter of claim the transmit filter of claim 34 wherein said sample generating circuitry generates samples on randomly selected cycles of said reference clock. Claim 35 depends from Claim 34 and is therefore allowable for the same reasons set forth above for the allowance of Claim 34.

Claim 36 further defines the transmit filter of claim the transmit filter of claim 34 wherein said sample generating circuitry generates samples on deterministically selected cycles of said reference clock. Claim 36 depends from Claim 34 and is therefore allowable for the same reasons set forth above for the allowance of Claim 34.

Applicants appreciate the Examiner's determination that Claims 5-15 and 22-31 would be allowable if amended to included the limitations of the base claim and any intervening claims, but believe in light of the above arguments that these claims are allowable in their present form. Claims 1-36 stand allowable over the references of record. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

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